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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,871	09/22/2003	Yee-Chia Yeo	TSM03-0553	1170

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,871	YEO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *60-89* is/are pending in the application.

4a) Of the above claim(s) *64, 76-79* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *60-63, 65-75, 80-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/2005, 6/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 60-61, 63, 65-66, 75, 80-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak et al. (U.S. Patent No. 6,100,153) in view of Yu et al. (U.S. Patent No. 6,784,101).

In re claim 60, Nowak et al. disclose the method of forming a resistor the method comprising:

forming a resistor body (12) of a first conductivity type in a portion of the silicon layer;

forming a dielectric layer (not labeled) overlying the body region

forming a top electrode (18) on the dielectric layer, the top electrode comprising a conductive material (doped polysilicon); and

forming a pair of doped regions (See Figure 1, and column 1, lines 55-65) of the first conductivity type oppositely adjacent the body region.

Nowak et al. does not disclose in the first embodiment the method of forming the resistor on a silicon-on-insulator substrate that includes a silicon layer overlying an insulator layer. Nowak et al. discloses the method of forming a resistor on a silicon-on-

insulator substrate that includes a silicon layer overlying an insulator layer or a bulk silicon substrate in a second embodiment (see column 4, lines 10-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a SOI substrate in the first embodiment of Nowak et al. because as Nowak et al. discloses bulk and SOI substrates are interchangeable. Further the examiner notes that SOI has particular advantages over that of bulk semiconductor wafers. SOI allow for reduction of the floating body effect and the area required for isolation between devices on an SOI wafer is less than the area typically required for isolation on a bulk silicon wafer.

Nowak et al. do not disclose the method wherein the dielectric layer comprises a material with a relative permittivity greater than about 8.

Yu et al. disclose the dielectric layer for a gate comprising a material with a relative permittivity greater than about 8 (see column 7, line 60 through column 8 line 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate of Nowak et al. by the method of Yu et al. to form a high k dielectric layer because it allows for greater device speed with less gate-to-channel leakage current such that there is overall improved device performance (see Yu et al. column 2, lines 4-30).

In re claim 61, Nowak et al. disclose the method wherein forming the resistor body comprises: forming an active region (12); forming isolation regions (24)

surrounding the active region; and doping the active region (52, see Figure 1 and column 1, lines 55-65).

In re claim 63, the combined Nowak et al. and Yu et al. disclose the method wherein forming the dielectric layer comprises a chemical vapor deposition step (see Yu et al. column 7, lines 45-60).

In re claim 65, the combined Nowak et al. and Yu et al. disclose the method wherein forming the dielectric layer comprises: forming an interfacial oxide, and forming a high permittivity dielectric layer (see Yu et al. column 7, lines 25-45).

In re claim 66, Nowak et al. disclose the method as claimed and rejected above, but does not disclose the method wherein forming the pair of doped regions comprises: doping a portion of the silicon layer not covered by the top electrode, forming spacers on sidewalls of the top electrode and doping a portion of the silicon layer not covered by the top electrode and spacers.

Yu et al. disclose the method wherein forming the pair of doped regions comprises: doping a portion of the silicon layer not covered by the top electrode, forming spacers on sidewalls of the top electrode and doping a portion of the silicon layer not covered by the top electrode and spacers (see column 8, lines 20 through column 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the source drain regions of Nowak et al. by the method of Yu et al. in order to form self-aligned source drain regions with extension regions that reduce leakage current.

In re claim 75, Nowak et al. disclose the method wherein the top electrode comprises a semiconductor (see column 1, lines 10-15).

In re claims 80-82, the combined Nowak et al. and Yu et al. disclose the method wherein the dielectric layer comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, and zirconium silicate, and combinations thereof and wherein the dielectric layer ahs a relative permittivity of larger than about 20 (see Yu et al. column 7, line 60 through column 8, line 10).

In re claims 83-85, the combined Nowak et al. and Yu et al. disclose wherein the dielectric has a physical thickness greater than about 40 angstroms (see Yu et al. column 2, lines 25-38 and column 7, lines 45-60).

In re claim 86-89, the combined Nowak et al. and Yu et al. do not disclose the method wherein the electrode has a width greater than about 0.1 microns or 1 micron or the electrode has a length greater than about 0.1 microns or 1 micron. The examiner notes that Applicant does not teach that the claimed dimensions solve any stated problem or are for any particular purpose. Therefore, the claimed dimensions range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrode with a width and length of greater than one micron to form a device with the desired resistance, and because it has been held

that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak et al. (U.S. Patent No. 6,100,153) and Yu et al. (U.S. Patent No. 6,784,101) in view of Eklund et al. (U.S. Patent No. 5,656,524).

In re claim 62, Nowak et al. and Yu et al. disclose the method as claimed and rejected above, but do not disclose doping the active region employs an ion implantation with a dose in the range of about 10^{13} to about 10^{16} cm^{-2}.

Eklund et al. disclose doping the active region employs an ion implantation with a dose in the range of about 10^{13} to about 10^{16} cm^{-2} (see column 4, lines 38-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implant with a dose in the range of about 10^{13} to about 10^{16} cm^{-2} because as Eklund et al. teach, it allows one to obtain the desired sheet resistance.

Claims 68-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak et al. (U.S. Patent No. 6,100,153) and Yu et al. (U.S. Patent No. 6,784,101) in view of Bohr (U.S. Patent No. 6,686,247).

In re claim 68, the combined Nowak et al. and Yu et al. disclose the method as claimed and rejected above, but do not disclose the method further comprising depositing an etch-stop layer over the top electrode and the spacers, forming an

interlayer dielectric over the etch-stop layer, forming contact holes in the interlayer dielectric layer, and filling the contact holes with a conductive material to form contact plugs.

Bohr discloses the method further comprising depositing an etch-stop layer over the top electrode and the spacers (224), forming an interlayer dielectric (226) over the etch-stop layer, forming contact holes (260, 270) in the interlayer dielectric layer, and filling the contact holes with a conductive material (260, 27, see Figure 4 and column 4, lines 44-65) to form contact plugs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the etch stop layer, interlayer dielectric layer and filling the contact holes in order to create electrical connections to provide a highly integrated circuits while preventing shorts.

In re claim 69, the combined Nowak et al., Yu et al. and Bohr disclose method wherein the etch stop layer comprises silicon nitride (see Bohr, 224, see column 3, lines 55-60).

In re claim 70, the combined Nowak et al., Yu et al. and Bohr disclose the method wherein the interlayer dielectric comprises silicon oxide (see Bohr, 226, see column 3, lines 55-60).

In re claim 71, the combined Nowak et al., Yu et al. and Bohr disclose the method wherein the first contact plug electrically contacts one of the pair of doped regions and a second contact plug electrically contacts the top electrode, said first and second contact plugs being electrically connected (see Figure 4).

Claims 67, 72-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak et al. (U.S. Patent No. 6,100,153) and Yu et al. (U.S. Patent No. 6,784,101) in view of Hwang et al. (U.S. Patent No. 5,273,915).

In re claim 67, Nowak et al. and Yu et al. disclose the method as claimed and rejected above, but do not disclose the method wherein the spacers are silicon nitride. Hwang et al. disclose the method of forming spacers of silicon nitride (see column 7, lines 1-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacers of the combined Nowak et al. and Yu et al. with silicon nitride because silicon nitride electrically isolates and is a known material for spacers, and it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

In re claims 72-74, Nowak et al. and Yu et al. disclose the method as claimed and rejected above, but do not disclose the particulars of the SOI wafer. Hwang et al. disclose the method wherein the insulator layer comprises silicon oxide, wherein the insulator layer has a thickness of less than about 1200 angstroms, and wherein the silicon layer has a thickness in the range of about 20 angstroms to about 1000 angstroms (see column 3, lines 10-20). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to form the device of the combined Nowak et al. and Yu et al. on the SOI wafer of Hwang et al. because the SOI wafer is conventional and because forming the resistor on the SOI has the advantages of extremely low parasitic capacitance due to full dielectric isolation and the insulating substrate.

Response to Arguments

Applicant's arguments with respect to claims 60-89 have been considered but are moot in view of the new ground(s) of rejection.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ng et al. disclose the dielectric layer for a gate comprising a material with a relative permittivity greater than about 8 (22, see [0039]). The examiner notes that Nowak et al. discloses it is desirable to form more than one component at a time and Ng et al. discloses that the method of using a high k dielectric for the resistor as well as the capacitor allow for eliminating masking steps while allowing for high capacitance for the capacitors (see [0028]).

.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk